Downscaling and Short Channel Effects in Twin Gate Junctionless Vertical Slit FETs

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Abstract—**In this work, we present the performance constraints in the design of ultra-thin body Junctionless Vertical Slit Field Effect Transistor (JL VeSFET). A design space that take into account the intrinsic off-current, the sub-threshold swing and the drain induced barrier lowering is investigated with respect to key technological parameters, namely, the doping level in the channel, the minimum slit width, and the effective radius of the slit. This work could serve as a guideline for technology optimization, design and scaling of JL VeSFETs.**

Index Terms—**Junctionless, VeSFET, DIBL, SCE, Design Space.**

I. Introduction

As CMOS technology is continuing its relentless downscaling, more and more challenges are faced in order to ensure sustainable fabrication costs of integrated circuits. Among various solutions that have been proposed by the research community, junctionless transistors have been investigated with an increasing interest in the last few years [1] [2]. While needing a much simpler and less expensive fabrication process thanks to the lack of junctions, these devices present performances that entitle them as good candidates for ultimate scaling, even down to 3 nm gate length [3], provided that the technological parameters are properly set [4].

Among different junctionless architectures, VeSFET is a new concept of transistor, introduced by Wojciech Maly [5] and demonstrated [6], that has the potential to alleviate the lithographic constraints by using highly regular arrays and to allow 3-D integration at nanometer scale. These devices can enable a new paradigm of integrated circuits (ICs), VeSTICs, for a lower manufacturing cost and fast design capabilities [7], [8]. They can be arranged in such a way that digital [9], [10] and analog [11] functions can be efficiently integrated upon a very regular layout. It has been demonstrated recently that single independent gate VeSFET can also act as "AND" and "OR" gates just by tuning the slit width, providing a 60% area saving in a NAND logic gate [7], [9]. Moreover, it has been shown that these devices present good characteristics for ultralow power / low frequency applications, outperforming bulk MOSFET and FinFET technologies [10], [12]. In addition to the junctionless architecture, the "vertical slit" topology can be applied also to junction-based and bipolar devices.

Today, the principle of operation has been proven [6] together with well controlled SCE for relatively large devices. However, there are still some technological limitations that have to be quantitatively assessed in order to optimize the device performance, while scaling down the dimensions. As for every other junctionless device, if the silicon layer of a VeSFET is too highly doped and/or too thick, it may become unfeasible to fully deplete the channel from electrons, whatever the applied gate voltage [13]. In addition, the doping level, N_D, affects the sub-threshold swing (SS) and can cause drain induced barrier lowering (DIBL).

Moreover, the particular topology of VeSFETs can add supplementary limitations to the performance, more precisely, the "shape" of the channel region. The actual slit radius is directly connected to the equivalent channel gate length of the device and, consequently, its value has an impact on the short channel effects.

Hence, from the designer's point of view, an in-depth simulation-based study is needed to propose a design space for JL VeSFETs. In Section II, we present the working principle of VeSFETs and explain the set of design parameters. Using TCAD simulations, in Section III we investigate the impact of doping level and slit radius on the electrical properties of the device, when a general downscaling is applied: the intrinsic off-current, SS, DIBL, and I_{on}/I_{off} ratio. Section IV presents in detail the impact that the channel region shape and dimensions have on SCE, also presenting measurements corroborating this analysis. The last section concludes the discussion, summarizing the results.

This work was funded by the Swiss National Science Foundation (SNF), project n° 200020_149822.

II. VeSFET Architecture

A typical layout of a VeSFET elementary cell is presented in Fig. 1. As introduced by [5], the dimensions of its geometric features (except the height H and the gate insulator thickness t_{ox}) are bounded by the key feature size r, which represents the radius of the minimum circle possibly achieved with the photolithographic process for a given technology node.

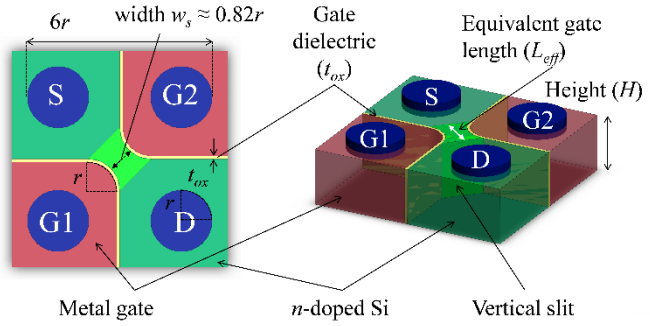


Fig. 1. The architecture of a single cell n-type VeSFET, as proposed in [5] for high density integration. Adapted from [16].

In a classical junctionless transistor as discussed in [1], the value of the effective gate length is very close to the physical gate length. Given that the channel height is constant, the charge depletion (when appropriate gate voltage is applied) is expected to be uniform throughout the entire channel length, when the drain to source voltage is low. Conversely, in the case of a VeSFET, the picture is much more complex due to the curved shape of the channel. While it is straightforward to fabricate long gate junctionless nanowires, VeSFET is intrinsically a short channel device, as soon as r is less than approximately 100 nm. The curved shape of the slit allows the depletion of the channel to take place only in a limited region between the source and the drain. For instance, in Fig. 1, the gate length is roughly identified as the "spread" of the region in light green color, which corresponds to a free carrier density of about 10^{16} cm^{-3}. From a simple geometrical analysis, it can be shown that the physical gate length could be expressed as

$$L_G = r_s\sqrt{2}\,, \tag{1}$$

where

$$r_s = r \tag{2}$$

is the radius of the slit curvature, equal to the key feature size r, as classically described for a VeSFET cell.

On the other hand, the technological parameters that play a critical role for switching off and for the on-current capabilities are the doping level (N_D) and the minimum channel thickness (here, w_s), as argued in [13]. In fact, it results that these two parameters are correlated: there is always a trade-off between the high on-state current (which needs high N_D) and the minimum slit width that the device should have in order to ensure full channel depletion (and therefore a reasonable off-state current). For high doping density, w_s should be relatively small, e.g., for $N_D = 10^{19}$ cm^{-3}, w_s should be less than 18 nm for an I_{on}/I_{off} ratio of at least five decades [13]. Given the relation that links r and w_s (Fig. 1)

$$w_s = 2r(\sqrt{2}-1) \cong 0.82r\,, \tag{3}$$

we note that the relative radius r would be less than 22 nm, dimension that could be more difficult to achieve and control during fabrication. We understand that downscaling VeSFETs with a general rule as in (1)-(3) means to decrease r, which gives consequently a smaller slit width and a shorter effective channel length. Notwithstanding better switching off capabilities, the device will also suffer from larger short channel effects.

With the decrease of r, the geometrical gate length will not match anymore with the "electrical" one that can be estimated from the depletion region when operating below the threshold. Given that the "electrical" length is much smaller than the geometrical, it becomes obvious that this definition is relatively unbalanced in VeSFET technology. In the next section we will show VeSFET behavior and performance when a general scaling rule is applied, i.e., r is scaled.

III. Electrostatics in JL VeSFET and Design Space

A. General considerations

Sentaurus Device (version 2009.06) has been used as TCAD simulation environment to define the three-dimensional device and to analyze the electrostatic behavior for all the scenarios presented in this work. The device height H is 5 nm and the gate oxide thickness t_{ox} is 2 nm. H is influencing the amount of drain current (in this work, always normalized to A/m) but it does not have a real impact on the performance of the device, as long as we consider the device walls (Fig. 1) being completely vertical. The impact of the oxide thickness is reported in [4]. The doping concentration is considered uniform through the channel and set to 10^{19} cm^{-3} while the source and drain regions are highly n-doped, 10^{20} cm^{-3}, to ensure ohmic contacts.

B. Electrostatics in VeSFET

The electrostatic potential distribution and the channel electron density for different values of radii are illustrated in Fig. 2. The drain and gate potential (with respect to the source) are 0.1V and -2.5V respectively. For the lowest radius considered here, i.e. $r = 10$ nm, we observed that when applying the lowest gate voltage (-2.5 V), the whole channel potential is decreased to about 90 mV, still following the gate voltage (not shown here) as there is full depletion of electrons in the silicon layer. However, when increasing the radius up to $r = 40$ nm, we see that the channel potential increase and ultimately reverts to its flat band value (in the center). In other words, the gate voltage value does not affect anymore the center potential for such a large silicon thickness, i.e. $t_{si,min} = 29$ nm (see Fig. 2.d). Therefore, the center potential remains almost neutral and the channel cannot be switched off anymore. This limitation is not a matter of gate voltage, but rather a phenomenon happening when an inversion layer of holes is generated at the channel interface, explained in [13] and experimentally observed in [14]. This layer screens the electric field and prevents any modification of the center potential.

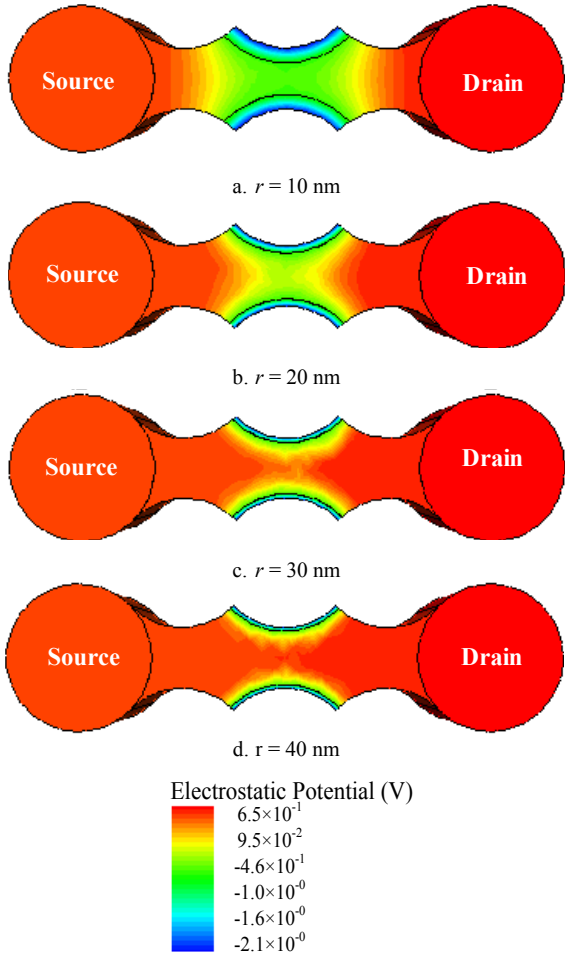


Fig. 2. Electrostatic potential distribution through the channel for different values of r in n-type junctionless VeSFET investigated in this work. The gate voltage is -2.5 V and the x and y dimensions are normalized to r = 10 nm. $N_D = 10^{19}$ cm^{-3}, $t_{ox} = 2$nm, $V_{DS} = 0.1$V.

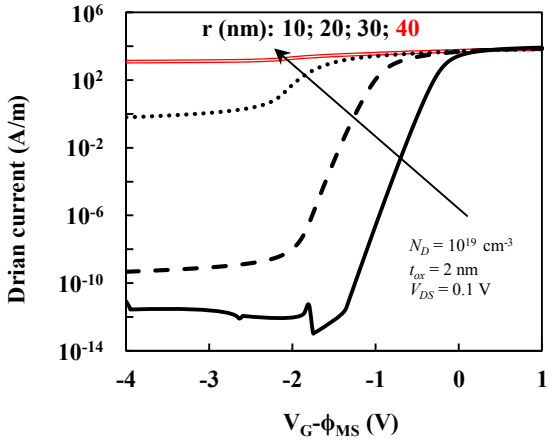


Fig. 3. I-V characteristics obtained with TCAD simulations for different radii, in n-type junctionless VeSFET investigated in this work.

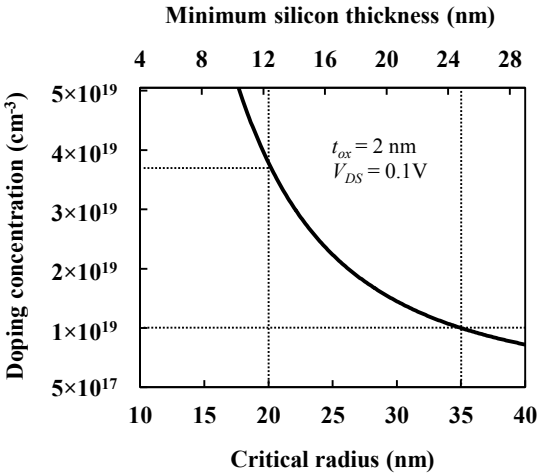


Fig. 4. Design space of n-type junctionless VeSFET. The curve represents the boundary where it becomes impossible to create a space charge in the center of the channel. The safe condition is fulfilled for the points below the curve.

I-V characteristics for highly doped channel (1×10^{19} cm^{-3}) obtained with TCAD simulations for different values of r are shown in Fig. 3. The values of all the currents are normalized to the device height and reported in A/m, for an easier comparison with different technology. As expected, for relatively thick silicon slits, the off-state current remains of the same order as the on-current. Based on this observation, we can propose a design space specific for the junctionless VeSFET where input parameters are the doping density and the slit radius.

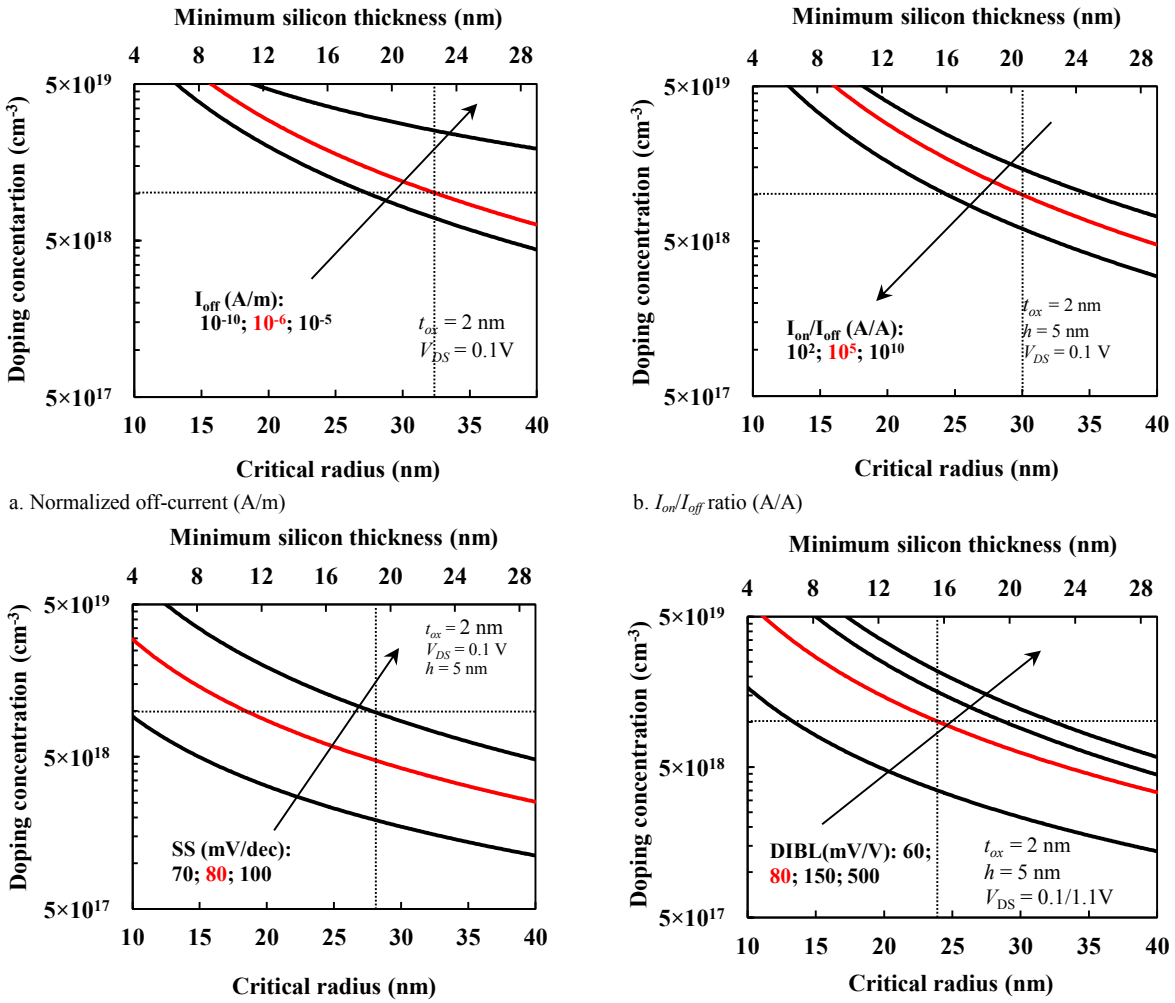
Fig. 4 displays the boundary where the center potential becomes "isolated" from the gate, i.e. when it becomes impossible to create a space charge depletion in the center of the channel. This clearly points out what are the technological conditions that will impede full depletion of the center of the channel, i.e., keeping the center of the slit neutral. For instance, for a doping density of 1×10^{19} cm^{-3}, the radius required must be less than 35 nm ($t_{si,min}$ = 24.7 nm). Otherwise, it will not be possible to deplete of electrons the center of the slit, not even by applying large negative voltages to the gate.

From a designer's standpoint, Fig. 4 is a first-level estimation of the channel doping concentration for a given radius. Obviously, the design space illustrated in the figure does not guarantee the lowest intrinsic off-current. In other words, inside this region of "safe operation", it is possible to achieve the depletion of electrons, but not the minimum leakage current. Hence, a simulation-based study on off-state current is necessary to estimate the intrinsic off-current for a certain doping density and radius.

C. Design space for general scaling of VeSFETs

1) Off-current and on/off-current ratio in JL VeSFET

So far, we pointed out some limitations to switch off VeSFETs in terms that are useful for the designer as such but only as a first approximation. Although the technological device parameters are situated below the frontier drawn in Fig. 4, we still need to assess what would be the order of magnitude for the off-state current and I_{on}/I_{off} ratio when the doping and the radius are known, since these currents are critical to design a JL VeSFET. The off-current is illustrated in Fig. 5a where the normalized pattern of the intrinsic off-current in JL VeSFET is



a. Normalized off-current (A/m)

b. I_{on}/I_{off} ratio (A/A)

c. Sub-threshold swing (mV/decade)

d. Drain induced barrier lowering (mV/V)

Fig. 5. Short channel effects of a VeSFET device, for different channel doping concentration (N_D) and slit radius (r), when general downscaling of the slit region is considered. a. – normalized off-current (A/m), b. – I_{on}/I_{off} ratio (A/A), c., sub-threshold swing (mV/decade) versus doping concentration (N_D) and radius (r) in a junctionless VeSFET.

shown with respect to the slit radius. As expected, the more doped the channel, the thinner the silicon must be to reduce the leakage current. For a given radius, the leakage current becomes larger when the doping density through the channel is increased.

The normalized on/off-current ratio in JL VeSFET (V_{DS} = 0.1 V) is illustrated in Fig. 5b. Similarly to I_{off} in Fig. 5a, the I_{on}/I_{off} ratio suffers a strong influence of the technological parameters, especially the minimum slit width. Choosing low doping and small radius seems optimum; however this also means that the on-state current will be small. Therefore, optimization will depend on the targeted application, whether it is low power or high speed.

2) Sub-threshold swing in JL VeSFET

Fig. 5c presents the influence of the slit radius and doping on the sub-threshold swing (SS). Unexpectedly, the simulations show that the doping concentration has a strong impact on the SS increase, suggesting also that lower doping is required to minimize this short channel effect. In order to satisfy an almost ideal sub-threshold swing of about 60 mV/decade, the doping density should be kept below 10^{18} cm^{-3}. Above this value, the slope is strongly affected by the slit radius. However, such a low doping density is not "aligned" to what has been reported for nanowires-based architectures in junctionless FET, as it might directly affect the on-current capabilities and time delay.

3) DIBL in JL VeSFET

Similarly, the drain induced barrier lowering, another relevant parameter to assess short channel effects, exhibits some dependence with the doping concentration. This is shown in Fig. 5d where we evidence that, similar to the SS, the DIBL becomes very large as soon as the doping level exceeds 10^{19} cm^{-3}, even for small slit radius. This leads to the conclusion that conversely to what is commonly adopted in JL nanowires, very high doping levels cannot be used in VeSFET technology unless relaxing the constraints on short channel effects.

IV. Impact of the Slit Radius

A. General considerations

In order to clearly separate the effect of the channel width with the one related to the channel radius, we will assume that the geometrical parameters w_s and r can be tuned independently, meaning that relations (2) and (3) are no longer used from now on. Therefore, we define an effective radius of the slit r_s as the local curvature of the channel, in the region where it is effectively controlled by the gate. Similarly, we define and investigate w_s as an independent parameter. We analyzed the impact of r_s on SCE for different w_s through TCAD simulations.

The structure and its technological parameters are identical to ones presented in the previous section, except the following changes: w_s and r_s are now assumed independent of r and the doping concentration through the channel is fixed to 5×10^{18} cm^{-3}. The key figure size r is fixed to 20 nm, and the height of the cell is 5 nm. The slit width is varied from 10 to 20 nm, a range that allows fully depletion and where quantum mechanical effects can still be neglected. The effective slit radius r_s is varied from 15 nm to 50 nm. Gate voltage sweeps were simulated at low (0.1 V) and high (1 V) drain to source voltage V_{DS}, to allow the extraction of drain induce barrier lowering (DIBL) and sub-threshold swing (SS).

B. Effective gate length

As it has been explained in Section II, it is difficult to evaluate precisely the equivalent gate length of a junctionless VeSFET due to the local curvature of the channel. The effective radius of the slit and its width are critical parameters besides the doping level. Given that the depletion depth propagates continuously along the gates, different values of gate voltages will result in different effective gate lengths. This is a direct consequence of the depletion depth dependence upon the gate voltage. Therefore, we propose to define the channel length by "measuring" the depletion in off-state when the drain current is about five decades lower than the on-state current (evaluated at flat-band and in saturation). A 2D layout of the mobile charge density is represented in Fig. 6 for two devices of interest, one with a local radius r_s = 15 nm and another with r_s = 50 nm.

When increasing the slit radius, the effective gate length is increased from 22 nm to 35 nm. It is therefore reasonable to affirm that when r_s is increased, VeSFET device behaves more similarly to a planar junctionless DG MOSFET.

The notion of "depleted channel" is not easy to define in terms of electron density inside the channel, as it depends on the assumed "threshold" value of mobile carrier. Fig. 7 presents three situations corresponding to different extensions of the depletion region. Depending on which threshold electron density is considered as "depleted channel", i.e., 10^{14}, 10^{15}, and 10^{16} cm^{-3}, we will arrive at different "electrical" gate lengths. The offset between these curves is constant for different slit radii (approximately 3.5 nm), even when the "threshold" electron concentration is changed by one order of magnitude, which is reasonable and still gives the correct trend for the "electrical" channel length dependence upon the parameters.

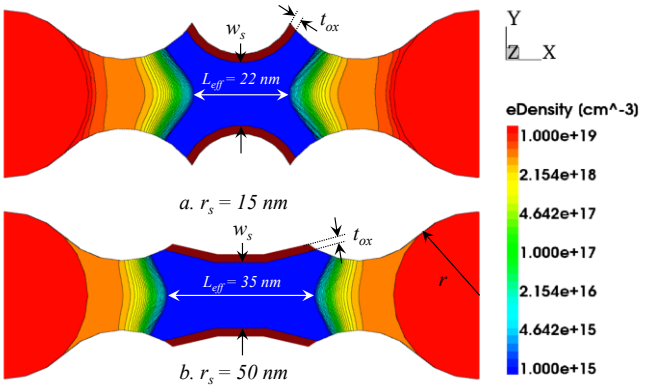


Fig. 6. Extraction of effective gate length at low V_{DS}, in sub-threshold regime, where the drain current is five decades lower than the on-state current (V_G = -1.4 V). The source and drain contacts (the red circular areas at left and right) are n-doped 10^{20} cm^{-3} although the scale saturates at 10^{19} cm^{-3}. The channel doping is 5×10^{18} cm^{-3} and the w_s is 15 nm.

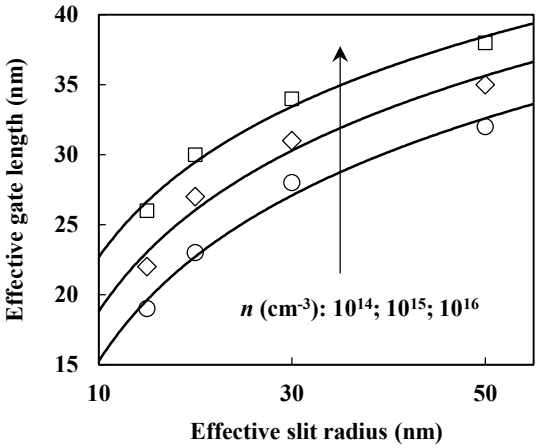
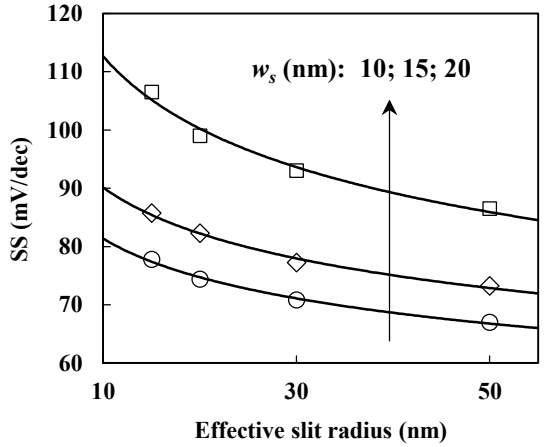


Fig. 7. Variation of the effective 'sub-threshold' gate length, as a function of the slit radius. The extraction is done at a V_G where the drain current is about five decades below the on-current. Lines are logarithmic (base 10) interpolation.

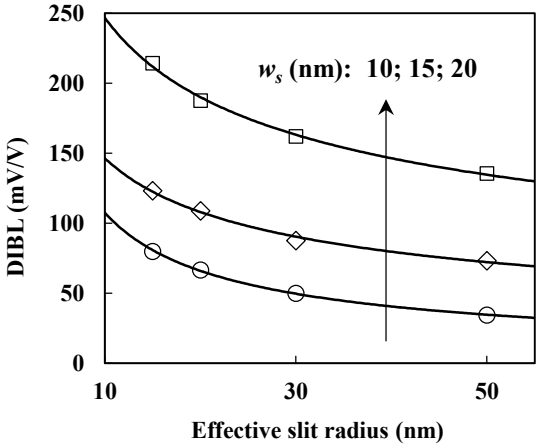
C. SCE: SS and DIBL

As it has been shown in the previous section, in VeSFETs short channel effects become more significant as the doping of the channel increases. This is a result of the lower depleting capability combined with the curved shape of the gates, which leads finally to a shorter channel. It means that, if there is any mean to "elongate" the channel while the dopant concentration is fixed, the SCE can be alleviated. In fact, this can be obtained by considering a larger slit radius, as in Fig. 6b.

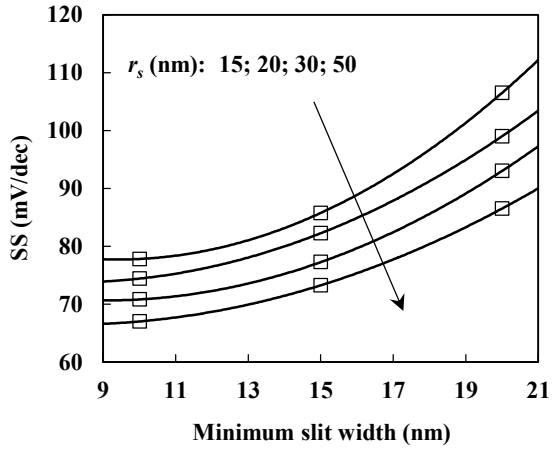
For different slit widths, Fig. 8a-b shows the improvements in terms of sub-threshold swing when changing the slit radius, passing from a small value of r_s to a larger one. When the radius r_s is increased from 15 nm to 50 nm, SS decreases by 13, 15 and 19% for a slit width of 10, 15, and 20 nm respectively. Note that w_s = 20 nm is already an extreme case, at the limits of a "successful" switching-off of the channel. This also explains the



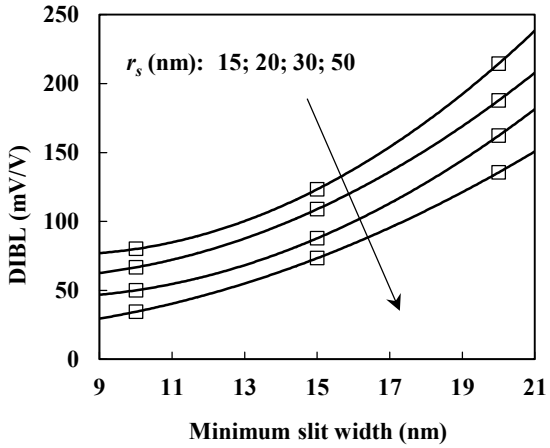
a. Impact of the effective slit radius on the sub-threshold swing



c. Impact of slit radius on the DIBL



b. SS of VeSFET as function of the minimum slit width



d. Impact of slit minimum slit width on DIBL, for different effective radii

Fig. 8. Short channel effects of a VeSFET device *n*-type doped 5×10^{18} cm^{-3} for different minimum slit widths (w_s) and radii (r), when downscaling is independently applied to considered separately for w_s and r

quite larger value of SS, as compared with the 15 and 10 nm widths.

The impact of the slit radius on the DIBL is shown in Fig. 8c-d. Here, the effect of r_s is even more significant than in the case of the SS. DIBL is decreased from 80 to 34 mV/V (-57%) for the 10 nm slit width, and from 214 to 136 mV/V (-36%) for the 20 nm slit width. Note that Fig. 8b and Fig. 8d present the same simulation results as in Fig. 8a and Fig. 8c, respectively, when the slit width is varied, which highlights the much higher sensitivity of SCE on the minimum silicon slit width compared to the local curvature.

For both SS and DIBL, it is reasonable to imagine that the extreme case of improvement ($r_s >> 1$) would lead to the same behavior as in the case of junctionless DG MOSFET [13].

D. SCE in fabricated devices

Single VeSFET devices have been fabricated at CMi (Center of Micro and Nano Technology) EPFL, following a technology process locally developed [15]. Devices with minimum slit width as thin as approximately 10 nm have been integrated on SOI substrates, uniformly *n*-doped by phosphorous at approximately 5×10^{18} cm^{-3}. Fig. 9 shows transfer characteristics of devices having the same slit width, approximately 10 nm, but

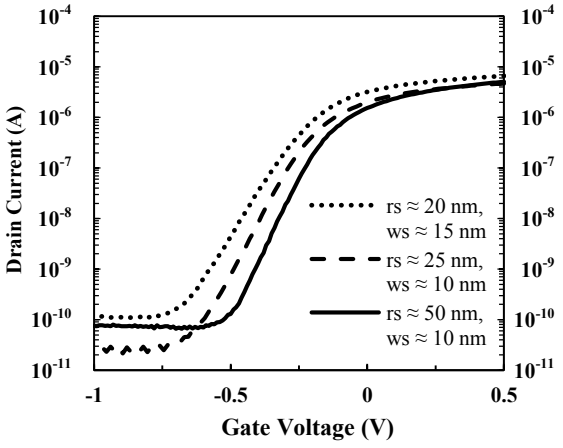


Fig. 9. Transfer characteristics of fabricated devices, with similar widths and different effective radius of the slit ($w_s \approx 10$ nm, continuous and dashed curves) or similar radii but different slit widths (dashed and dotted curves)

different slit curvatures, about 25 and 50 nm (the continuous and the dashed curves). The difference when having similar slit curvature but different widths can be noted comparing the dashed curve with the dotted one. The effect of different slit radii and slit widths is evident, resulting in larger SS and a lower threshold voltage, which confirms that these parameters should be controlled accurately, for low SCE.

V. Conclusion

We investigated in details the design space of junctionless VeSFETs in terms of short channel effects by means of extensive TCAD numerical simulations. This study shows that the choice of optimum technological parameters depends on the targeted application. Furthermore, it is shown that despite the fact that high doping provides a good on-current level, it leads to the increase of short channel effects. Considering a slit shape with a larger radius can alleviate the decrease in performance by elongating the effective gate length. All this constrains should be considered when designing analog and digital circuits based on VeSFET devices.

Acknowledgements

The authors would like to thank Prof. Wieslaw Kuzmicz and Prof. Wojciech Maly for introducing them to the VeSFET concept.

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